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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,899	05/15/2001	Hendrik Rotsch	A34306	1159

7590 03/17/2005

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EXAMINER	
DEPPE, BETSY LEE	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,899	ROTSCH ET AL.	
	Examiner	Art Unit	
	Betsy L. Deppe	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *three*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2001 and 02 November 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on November 2, 2004. These drawings are not approved because the replacement sheets are not labeled with "Replacement Sheet."

2. The drawings are objected to because Figure 3 show counter 15 as being inside PLL 6 while Figure 2 shows counter 15 external to PLL 6. If the counters in Figures 2 and 3 are referring to different counters then a different reference number should be used for clarification.

Specification

3. The disclosure is objected to because of the following informalities: the first sentence in paragraph [0036] on page 12 is inconsistent with Figure 3. Paragraph [0036] describes stable clock signal Z as being produced by the phase regulator and refers to it as "b." However, in Figure 3, stable clock signal Z is produced by ***counter 10*** and the output of the phase regulator 5 is identified as "***d***." Appropriate correction is required.

Claim Objections

4. The claims are objected to because of the following informalities:

   a. in claim 1, line 6 and claim 7, line 3, "a stable number of clock signals" should be "stable clock signals" in order to be consistent with the terminology subsequently used (for example, see claim 1, lines 8 and 13 and claim 7, line 5);

b. in claim 1, lines 10-11 and claim 7, line 7-8, "between said first clock transmitter and said second clock transmitter" should be "between said **stable clock signals** and said second clock **signals**" since "phase differences" occur between signals, not transmitters. Similarly, the following occurrences of "second clock transmitter" should be "second clock **signal**": two occurrences in claim 1, line 12; claim 2, line 2; and claim 7, lines 9 and 11;

c. in claim 4, line 2, "said first stable clock signals" should be "said stable clock signals";

d. in claim 6, line 3, "said stable clock signal" should be "said stable clock **signals**";

e. in claim 7, line 10, "said first clock transmitter" should be "said **stable clock signals**" and "said phase regulator" should be "**a** phase regulator."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 2 and 4-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. With regard to claims 1, 2, and 4-6, it is unclear what is meant by "such that a shorter interval between phases of said stable clock signals and said second clock signal are reduced" in claim 1, lines 13-14. For example, is the phase difference

between the stable clock signals and the second clock signal reduced? Furthermore, what is the "shorter interval" referring to?

8. With regard to claims 7 and 8, in claim 7, lines 9-11, it is unclear whether the fluctuations of the period duration of the stable clock signals are mapped onto the second clock signal or whether the corrected stable clock signal is mapped onto the second clock transmitter. Paragraph [0044] suggests that the fluctuations of the period duration of the stable clock signals are mapped onto the second clock signal whereas paragraph [0048] suggests that a corrected signal is mapped onto the second clock signal.

Claim Rejections – 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai et al. (US Patent No. 5,003,559, cited in the Office Action mailed September 3, 2004) in view of Southard (US Patent No. 4,598257, cited in the Office Action mailed September 3, 2004).

11. With regard to **Claim 1**, Kanai et al. discloses a digital transmission system (method) with the transmission unit transmitting synchronization signals (see figures 3 and 5A-57; col. 2, lines 4-15; col. 3, lines 4-15) to a reception unit; the receiver

extracting the received synchronization signals; and supplying it to a clock generator [transmitter] that outputs a stable number of jitter-free (col. 3, line 30) clock signals, with predetermined frequency, and phase-locked with [and between two] synchronizing signals (col. 2, lines 16-36; col. 3 lines 16-20; col. 5, line 21 to col. 6, line 3) [because, the fact that each clock generation starts with detection of a synch signal, means that the receiver clock generates a stable (constant) number of clock signals between two synch signals]; Kanai et al., however, fails to teach the use of a second clock generator [transmitter] that is driven by the first generated clock signal and that is continuously present even when the first clock signals are absent; neither does Kanai et al. teaches how and whether the second clock signal is phase synchronized with the first clock signal.

Southard teaches that since the signal transmitted from the master clock [in a transmitter] to a slave clock [in a receiver] is subject to wander (frequency variation) and jitter (phase variation) and may lose its integrity or disappear completely (col. 1, lines 62-65), the slave clock [in the receiver] must be equipped to discern the average frequency of the master [in the transmitter] clock signal and to take quick remedial action upon detection of failure (col. 1, line 68 to col. 2, line 5), and must be capable of being maintained on a routine basis, or repaired if a failure occurs, while maintaining a stable and synchronized [with the received reference clock] signal output. Southard also teaches that it is known to use a receiver (slave) clock comprising of at least two redundant [clock signal generating] units, operating in synchronization with each other and with the transmitted reference clock, so that one [clock signal generating] unit can be removed and maintained or repaired while the other unit continues to operate and,

ideally, being possible to switch from one of the two redundant clock units to the other while maintaining a constant frequency (slip free) and constant phase (glitch free) output signal (col. 2, lines 6-18). Furthermore, Southard discloses an apparatus that includes a first and a second clock generator (CCG) that operate in master and slave relationship, each clock generator unit comprising a controllable oscillator for generating and presenting a clock pulse signal and a device for controlling the oscillator so as to maintain the frequency of the clock pulse signal substantially constant (in the case where the subject clock generator is operating as a "master") or to cause the frequency and phase of this clock pulse signal to closely follow the frequency and phase of the clock pulse signal produced by the other clock generator (in the case where the subject clock generator is operating as a "slave") (col. 3, lines 26-39); further, the master CCG is operative either to produce a stable clock signal of its own or to follow the external reference clock signal, and the slave CCG operates to produce [using the stable clock signal being supplied to it by the first clock generator] an output clock signal which is identical in frequency and substantially identical in phase to the frequency and phase, respectively, of the output clock pulse signal produced by the master CCG (col. 3, lines 55-62). If the master CCG becomes faulty [absent], it is possible to reverse the master-slave relationship without the slightest phase slip or discontinuity in the output signal (col. 3, lines 66 to col. 4, line 7). Each CCG contains a microprocessor based intelligent phase lock loop (PLL) (col. 6, lines 47-49) and the slave CCG closely follows the frequency and phase of its master partner by executing its very accurate frequency and phase locking algorithm (col. 14, lines 22-27) and adjusts for the phase difference between its clock signal and the master CCG clock signal by changing the frequency of

the slave CCG clock signal (col. 16, lines 23-26). Changing the frequency of a clock signal implicitly changes the period duration of the clock signal. Based on the phase difference between the two signals, it is implicit that the period duration of the clock signal is either reduced or expanded to synchronize the signals thereby eliminating the phase difference.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. because incorporating the redundant CCG clock signal generating method of Southard into the Kanai et al. digital transmission method provides for a continuous and stable clock signal in the receiver unit that is synchronized with an extracted reference clock signal of the transmitter (an external reference clock) wherever an uninterrupted (and in synchronization with a transmitted synchronization instruction) data processing is needed.

12. With regard to **Claim 2**, claim 2 inherits the limitations of Claim 1; further, Southard teaches that the fine phase measurements are used as input to a proportional control path and an integral control path that are added together with the frequency offset function (coarse integral part) and the modulation function to control the voltage controlled crystal oscillator (col. 10, lines 35-42); and that the execution of a routine in the slave CCG changes the frequency of the slave CCG clock signal slightly so that the phase of this clock signal will drift with respect to the phase of the master CCG clock signal; and that this phase drift is allowed to continue for 1 second; the entire fine phase locking procedure should not exceed a prescribed maximum time period (col. 19, lines 51-54). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. for producing the claimed invention because incorporating the slight phase drift of the second (slave) CCG allows for fine (soft) synchronization.

13. With regard to **Claims 5 and 6**; claim 5 inherits the limitations of Claim 1. Southard also teaches that the first clock generator includes a control means that includes a digital phase comparator means for comparing the phase of the first clock pulse signal with the phase of a reference clock signal [the received clock signal; synchronization signals] and producing a first digital signal representative of the difference in phase; and a processing means comprising a digital microprocessor, connected to said first phase comparator means, for producing said first control signal in response to said first digital signal (col. 23, lines 55-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Southard into the method of Kanai et al. because supplying the synchronization signal (extracted transmitted clock signal) via a phase regulator (phase comparator and frequency controller) of a PLL provides means provides a stable clock signal that is synchronized with the received reference clock signal.

14. With regard to **claim 7**, Kanai et al. in view of Southard discloses the claimed invention including a first transmitter and a second transmitter, as recited. (See the rejections of claims 1 and 5 above for corresponding limitations.) Since the second clock transmitter uses the stable clock signals provided by the first clock transmitter, it is implicit that fluctuations or changes in the period duration of the stable clock signals impacts (i.e. "are mapped to") the second clock transmitter and its output signal.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai et al. in view of Southard as applied to claims 1 and 2 above, and further in view of Gegner et al. (US Patent No. 4565975, cited in the Office Action mailed September 3, 2004). Claim 4 inherits the limitations of Claim 1 or 2. However, Kanai et al. in view of Southard does not teach driving the second clock transmitter with a prescribed standard period duration if the stable clock signals are absent.

Gegner et al. discloses that a clock signal T2 is generated that is synchronous with the original sending pulse (in interference free operations), and is used for synchronously detection of the incoming digital signals (col. 5, lines 3-9). In the case of longer lasting interference [absence of the first clock pulse, or the synch signal], the oscillator VCO (using a reference voltage) generates the clock pulse T3 at a predetermined (nominal) frequency (col. 3, lines 37-42; col. 4, lines 27-29; col. 8, lines 37-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Gegner et al. into the method of Kanai et al. in view of Southard in order to ensure that the second clock transmitter continuously provides a clock signal if the stable clock signals are absent thereby avoiding a disruption of the system caused by the lack of a clock signal.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai et al. in view of Southard as applied to claim 7 above, and further in view of Finsterbusch et al. (DE 19932635, cited in the IDS filed May 6, 2003). Kanai et al. in view of Southard as applied to claim 7 above discloses the claimed invention except for the recited phase regulator. Finsterbusch et al. discloses the recited phase regulator. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the phase regulator into the circuit disclosed by Kanai et al. in view of Southard in order to generate a more stable clock signal by considering instantaneous phase errors.

17. Claims 1, 2 and 4-8 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Alder et al. (EP 0 652 642 A1, cited in the IDS filed May 6, 2003) in view of Finsterbusch et al.

18. With regard to claims 1 and 7, Figure 1 of Alder et al. discloses the claimed invention including a first clock transmitter (4) and a second clock transmitter (3) wherein the second transmitter (3) uses the stable clock signals provided by the first transmitter (4) to generate a second clock signal (v_0/N_1). (See the abstract) However, Alder et al. does not teach transmitting synchronization signals and outputting the stable clock signal between two of the synchronization signals.

19. Finsterbusch et al. teaches a circuit that generates clock signals between two of the synchronization signals. (See Figure 1) It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Finsterbusch et al. with that of Alder et al. in order to provide a circuit with greater control over the generation of the clock signals by using a synchronization signal. The synchronization signal may be used to trigger the generation of the clock signal at the desired time.

20. With regard to claim 2, Alder et al. in view of Finsterbusch et al. discloses the claimed invention including changing the phase difference between the stable clock signals and second clock signal. (See "20," "30," and "40" in Alder et al.)

21. With regard to claim 4, Alder et al. in view of Finsterbusch et al. discloses the claimed invention including driving the second clock transmitter with a prescribed standard period duration. (See V_{ref} in Alder et al)

22. With regard to claims 5, 6 and 8, Alder et al. in view of Finsterbusch et al. discloses the claimed invention including the phase regulator. (See "5" in Finsterbusch et al.)

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Betsy L. Deppe whose telephone number is (571) 272-3054. The examiner can normally be reached on Monday, Wednesday and Thursday (8:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272 - 2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Betsy L. Deppe
Primary Examiner
Art Unit 2637